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Senior Analog Ic Designer And Technical Advisor Resume

★★★★★ 2.00 /5 (Submit Your Rating)

SUMMARY

- 10+ Years Experience in Analog, RF and Mixed Signal IC Designs
- 12+ Years Experience as an Electronics Engineer in the Field of Microelectronics
- Comprehensive Knowledge of Analog/Digital Electronic Devices, Circuit Design Principles, and Experience in using Design/Analysis Tools
- Working Experience with a variety of Technologies such as Si and SiGe, GaAs, CMOS and BJT
- Good Knowledge of both Transistor - Level Design and System Level Design, Modelling, Specification, and Characterization
- Good Knowledge of VLSI (design, layout, processing & packaging), ASIC Design, FPGA Design, Telecom & Protocols
- Excellent Troubleshooting & Analytical Skills
- Outstanding Interpersonal & Team Skills

PROFESSIONAL EXPERIENCE

Confidential

Senior analog IC designer and Technical advisor

Responsibilities:

- Provided technical advice and support to the electronics engineers on IC designs, including analog, digital and RF IC designs.
- Ensured new IC designs and projects align with application needs and technical standards.
- Responsible for introduction of latest advances in IC design technologies

Confidential

Senior analog design engineer

Responsibilities:

- Designed different analog and digital regulators (LDO) with low noise and high PSRR on CMOS technology
- Designed different Schmitt Triggers with high speed and low power consumption on CMOS technology
- Designed low power (80 µ W), low voltage (1.2V) Sigma-Delta ADC on CMOS technology

Confidential

Senior analog IC designer

Responsibilities:

- D oing design research on new CMOS technology nodes such as 65nm, 45nm, 32nm and 22nm
- Designed 60GHz power amplifier and LNA on 90nm CMOS technology
- Designed low power wideband LNA on 0.1 3 µm CMOS technology for WiMAX application
- Designed 10 bit pipeline ADC (analog to digital converter) on 90nm CMOS technology for high speed, low voltage and low power consumption
- Designed low power (140 µ W), low voltage (1V) Sigma-Delta ADC on 90nm CMOS technology
- Designed high speed (100Ms/s, 4MHz bandwidth) Sigma-Delta ADC on 90nm CMOS technology
- Conducted the design of half rate (5- G B /s) CDR (Clock and Data Recovery Circuit) for optical receivers using 0. 18 µm CMOS technology
- B e engaged in the design of PLL on 0.35 µm CMOS technology

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